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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,593	10/02/2006	Nikil Dutt	703538.4054	1321
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ORRICK, HERRINGTON & SUTCLIFFE, LLP			WANG, JUE S	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/599,593	DUTT ET AL.	
	Examiner	Art Unit	
	JUE WANG	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 02 October 2006.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-27 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 02 October 2006 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. _____.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 10/2/2006.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application

6) Other: _____.

DETAILED ACTION

1. Claims 1-27 have been examined.

Claim Objections

2. Claim 6 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Claim 6 contains the same limitation as parent claim 5. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 12-27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

5. Claims 12-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In claims 12-23, a “generic instruction model” is recited; however, it appears that the generic instruction model would reasonably be interpreted by one of ordinary skill in the art as software, per se, since the instruction specification and operation classes recited as part of the generic instruction model would reasonably be interpreted by one of ordinary skill in the art as software, per se. As such, it is believed that the generic instruction

model of claims 12-23 is reasonably interpreted as functional descriptive material, per se, failing to be tangibly embodied or include any recited hardware as part of the generic instruction model and thereby fit that statutory category of invention.

6. Claims 24-27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In claims 24-27, a “computer readable medium” is recited; however, there is no explicit definition in the specification for the “computer readable medium”. It should be known that “air”, “wireless transmission”, and the like are computer readable medium, but are non-statutory claim subject matters. Accordingly, the “computer readable medium” as recited in claims 24-27 is not limited to that which falls within a statutory category of invention because the specification fails to limit “computer readable medium” to embodiments which fall within a statutory category. To overcome the 101 rejection, applicant is suggested to either amend the specification with an explicit definition of “computer readable medium” excluding non-statutory embodiments or to add the limitation “non-transitory” to the claims.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Reshadi et al. “A Framework for Fast, Flexible and Retargetable Instruction-Set Architecture Simulation” (hereinafter Reshadi).

9. As per claim 1, Reshadteaches the invention as claimed, including a method of simulating an instruction set architecture (ISA) with a instruction set simulator (ISS), comprising:

fetching a first decoded instruction during a run time (i.e., engine fetches the decoded instructions from the instruction memory, see page 6, paragraph 1), wherein the decoded instruction is decoded from an original instruction in a target application program during a compile time preceding the run time (i.e., the static instruction decoder decodes the target program, then generates the optimized source code of the decoded instructions, the decoded instructions are compiled on the host machine, see page 5, paragraphs 2, 3, page 6, paragraph 1, page 10, last paragraph, page 11, paragraph 1), the decoded instruction pointing to a template configured to implement the functionality of the instruction (i.e., the decoded instruction is executed using an execution function where the execution functions include templates, see page 6, paragraph 1, page 11, paragraph 3, page 12);

determining whether the fetched instruction is modified from the original instruction (i.e., if the simulator detects that the program code of a previously executed address has changed, see page 5, Figure 2, page 6, paragraph 1, page 11, paragraph 1); and

executing the designated template if the instruction was not modified (i.e., the decoded instruction is executed using an execution function where the execution functions include templates, see page 6, paragraph 1, page 11, paragraph 3, page 12).

10. As per claim 2, Reshadteaches decoding the original instruction by selecting a template corresponding to the original instruction and customizing the template based on the data in

original instruction prior to fetching the instruction (i.e., the DetermineTemplate function returns the DataProcessing template for this binary instruction, see page 11, first paragraph, page 12, last paragraph).

11. As per claim 3, Reshadi teaches wherein the template corresponds to a first class of one or more instructions and wherein the template has a corresponding mask usable to identify instructions belonging to the first class (i.e., we define a set of masks for each instruction class, we use C++ templates to implement the functionality for each class of instructions, see page 12, paragraph 2).

12. As per claim 4, Reshadi teaches wherein selecting a template comprises: comparing the original instruction to the mask corresponding to the template; and selecting the template if the mask matches the original instruction (see page 12, paragraph 2).

13. As per claim 5, Reshadi teaches wherein customizing the template comprises determining a value of a parameter in the template based on the data in the original instruction (see page 12, paragraphs 2-4).

14. As per claim 6, Reshadi teaches wherein customizing the template comprises determining a value of a parameter in the template based on the data in the original instruction (see page 12, paragraphs 2-4).

15. As per claim 7, Reshadi teaches compiling a first program comprising the customized template in the compile time (see page 11, Figure 5, page 12, last paragraph, page 13, Figure 6).

16. As per claim 8, Reshadi teaches optimizing the template during the compile time (see page 13, Figure 6, paragraphs 2, 3).

17. As per claim 9, Reshadi teaches re-decoding the fetched instruction during the run time if the fetched instruction was modified, wherein the re-decoded instruction designates a function configured to implement the functionality of the instruction; and executing the designated function if the instruction was modified (see page 5, Figure 2, page 6, paragraph 1, page 11, paragraph 1).

18. As per claim 10, Reshadi teaches executing the modified instruction using an interpretive process (see page 10, last paragraph, page 11, paragraph 1).

19. As per claim 11, Reshadi teaches compiling the target application program to generate the original application (see page 10, last paragraph, page 11, Figure 5, paragraph 1).

20. As per claim 12, Reshadi teaches the invention as claimed, including a generic instruction model for use in instruction set architecture (ISA) simulator, comprising:

an instruction specification usable to interpret each instruction in an ISA (see page 5, paragraph 2), the instruction specification comprising one or more operation classes (see page 6, paragraph 6);

wherein each operation class defining a set of one or more instructions (i.e., an operation class refers to a set of similar operations in the instruction set, see page 6, paragraph 7), the operation class having an operation mask usable to identify instructions belonging to the class (see page 6, paragraph 4); and

further wherein the operation class comprises one or more symbols and an expression describing the class in terms of the one or more symbols (i.e., an operation class is composed of a set of symbols and an expression that describes the behavior of the operation class in terms of the values of its symbols, see page 6, last paragraph), each symbol having a corresponding set of one or more symbol types (i.e., each symbol may be a different type, see page 6, last paragraph), each symbol type in the set comprising information usable to determine the symbol when compared to an instruction (see page 7, paragraph 2).

21. As per claim 13, Reshadi teaches wherein the set of instructions has a common behavior (i.e., an operation class refers to a set of similar operations in the instruction set, see page 6, paragraph 7) and the expression defines the behavior of the class in terms of the one or more symbols (i.e., an expression that describes the behavior of the operation class in terms of the values of its symbols, see page 6, last paragraph).

22. As per claim 14, Reshadi teaches wherein one symbol type in the type set is an constant type (see page 7, paragraph 2).

23. As per claim 15, Reshadi teaches wherein the type set comprises a plurality of constant types (i.e., integer, boolean, float, see page 8, paragraph 1), each constant type having a corresponding type mask usable to determine the constant when compared to an instruction (see page 7, paragraph 2, page 8, paragraph 1).

24. As per claim 16, Reshadi teaches wherein one symbol type in the type set is a register type (see page 7, paragraph 2).

25. As per claim 17, Reshadi teaches wherein the register type comprises a register index and a register class (see page 7, paragraph 4).

26. As per claim 18, Reshadi teaches wherein one symbol type in the type set is an operation type (see page 7, paragraph 2).

27. As per claim 19, Reshadi teaches wherein the type set comprises a plurality of operation types, each operation type having a corresponding type mask usable to determine the operation when compared to an instruction(see page 3, Figure 3, page 8, paragraph 2).

28. As per claim 20, Reshadi teaches wherein at least one operation class comprises a plurality of expressions, each expression being conditional on data within an instruction (see page 6, paragraph 3, page 7, Figure 3).

29. As per claim 21, Reshadi teaches wherein each instruction comprises a series of slots, each slot comprising data translatable into an operation (see page 6, paragraph 5).

30. As per claim 22, Reshadi teaches wherein each instruction comprises a series of binary data values and the operation mask comprises a series of mask positions wherein each mask position corresponds to one instance of a binary data value (see page 6, paragraph 4).

31. As per claim 23, Reshadi teaches wherein each mask position has a value selected from a group comprising: a binary one value, a binary zero value and a do not care value. (see page 6, paragraph 4, page 8, paragraph 4).

32. As per claims 24, 26, and 27, these are the computer readable medium claims of claims 1, 9, and 10. Therefore, they are rejected using the same reasons as claims 1, 9, and 10.

33. As per claim 25, Reshadi teaches wherein the template corresponding to a first class of one or more instructions and wherein the template has a corresponding mask usable to identify instructions belonging to the first class (see page 12, paragraph 2).

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Sanyal et al. (US 7,607,120 B2) is cited to teach method and apparatus for creating data transformation routines for binary data.
- Nevill et al. (US 2002/0066003 A1) is cited to teach restarting translated instructions.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jue S. Wang whose telephone number is (571) 270-1655. The examiner can normally be reached on M-Th 7:30 am - 5:00pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on 571-272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193

Jue Wang
Examiner
Art Unit 2193